

AISHWARYA PANCHAL

P.C.B. Designer

Contact

Address

Bengaluru, India

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Technical Profile

- Altium Designer (V 23.1.1)
- PCB Designing
- Design Rule Checking (DRC)
- Footprint creation
- Product Placement
- Routing Protocols
- Schematic creation
- Symbol Creation
- Placement
- Layout Guidelines
- DRC Checking
- DFM
- Constraint Setting
- Bill of Materials (BOM) Management
- Gerber Generation
- Footprint QC Checking

Academic Project

1. Touch less doorbell
2. Waste segregation system using IOT.

Languages

- English
- Kannada
- Hindi

A highly motivated and detail-oriented PCB Design Engineer with a strong foundation in PCB development and a passion for innovative solutions. Seeking a challenging role that leverages expertise in system design, IT administration, networking, and hardware to contribute to the company's strategic and operational success. Skilled in multitasking and organization, with a proven ability to handle complex projects efficiently and effectively.

Experience

PCB Designer

Dec-2023 to Jan-2025
Drivi Silicon, Bengaluru.

- Addressed design challenges and evaluated alternative design models to meet project requirements.

Internships

Sep-2023 to Oct-2023
Academic Internship
CITL, Bengaluru.

Education

Bachelor of Engineering

Basavakalyan Engineering College

Branch: Electronics and Communication.

Y.O.P: 2023

Pre University College

Basavathirtha Comp PU college

Y.O.P: 2019

SSLC

S.E.S. Gouribai Agarwal Girls Jr. College

Y.O.P: 2017

Projects

1. LEXI_R10_M.2_KEY_E
2. PROGRAMMING_ADAPTOR
3. DOME_INTERFACE
4. DTS_NORA_W30 SERIES REV_1P0